said memory further comprising a plurality of word lines and a plurality of plate lines distinct from said bit lines and word lines, each of the memory cells being coupled to a word line, each memory cell being coupled also to a plate line, each plate line being coupled to a capacitor plate electrode of a cell, and

each said memory cell further including a respective switching device located within the memory cell, said first plate electrode of said capacitor in said cell being coupled to one said bit line via said switching device, said switching device being coupled to be controlled by one said word line, said second plate electrode of said capacitor in said cell being coupled to one said plate line.--

--73. In a nonvolatile ferroelectric memory of the type having a plurality of memory cells arranged in rows and columns, each column comprising a bit line coupled to memory cells along the column, each said memory cell comprising a ferroelectric capacitor having first and second plate electrodes, the polarization of said capacitors corresponding to the data stored therewithin, the improvement wherein:

said memory further comprises a plurality of word lines and a plurality of plate lines distinct from said bit lines and word lines, each of the memory cells along a row being coupled to a word line corresponding to the row, each memory cell being coupled also to a corresponding plate line, each plate line being coupled to plate electrodes in a plurality of said cells,

each said memory cell further including a respective switching device located within the memory cell, said first plate electrode of said capacitor in said cell being coupled to its corresponding bit line via said switching device, said switching device being coupled to be controlled by said

corresponding word line, said second plate electrode of said capacitor in said cell being coupled to said corresponding plate line.--

--74. A non-volatile ferroelectric memory comprising an array of memory cells arranged in rows and columns, each said row corresponding to a respective word line, each said column corresponding to a respective bit line,

a respective sense amplifier coupled to each said bit line;

each memory cell comprising a ferroelectric capacitor having first and second plate electrodes and a transistor located within said cell for coupling said first electrode of said ferroelectric capacitor to the corresponding said bit line;

said word line being coupled to a control electrode of said transistor; and

a plate line coupled to the second plate electrode of said ferroelectric capacitor, said plate line being coupled to second plate electrodes of a plurality of capacitors in said array, said plate line being distinct from said word lines and said bit lines.--

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REMARKS

Pursuant to Rule 1.607, Applicants hereby request that an interference be declared between the above-referenced application and U. S. Patent No. 4,873,664, by Eaton, Jr., which patent issued October 10, 1989.

The proposed count is set forth below:

THE COUNT

In a nonvolatile ferroelectric memory of the type having a plurality of memory cells, a bit line coupled to each said memory cell, each said memory cell comprising a ferroelectric capacitor having first and